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TITLE: Deposition film surface treatment method used during semiconductor device manufacture, involves performing plasma etching process using mixed gas of chlorine and oxygen, hydrogen bromide

PRIORITY-DATA: 2000JP-0219562 (July 19, 2000)

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Masamichi et al.

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
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INT-CL (IPC): H01 L 21/28; H01 L 21/3065; H01 L 21/3205; H01 L 21/3213; H01 L 29/43

ABSTRACTED-PUB-NO: JP2002043284A

BASIC-ABSTRACT:

NOVELTY - A silicon deposition film is processed using hydrogen bromide (HBr), and the mixture of chlorine gas and oxygen gas. The mixing rate of oxygen and chlorine is 0.5-30%.

USE - For performing etching process of silicon deposition film on surface of semiconductor element used during semiconductor device manufacture.

ADVANTAGE - The side wall of the n-type gate electrode pattern is protected during the plasma etching process, hence surface treatment is performed with high accuracy.

DESCRIPTION OF DRAWING(S) - The figure explains a sectional view of the plasma etching process.

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PATENT ABSTRACTS OF JAPAN

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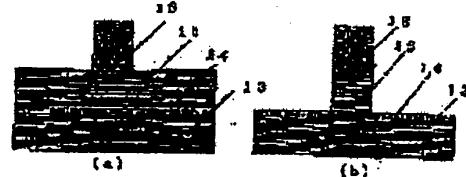
(54) STACKED FILM SURFACE TREATING METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a stacked film surface treating method capable of treating a stacked silicon film with anisotropy and high precision when treating it with a plasma etching device.

SOLUTION: Treatment is divided into several steps until exposing a gate oxide film 14 and for removing residue on the side wall of a gate electrode polycrystal silicon part 15 and the film 14. Plasma etching using gaseous hydrogen bromide (HBr) or mixed gas containing hydrogen bromide (HBr) is performed in at least one step in a former half and plasma etching using mixed gas of chloride (Cl₂) and oxide (O₂) is performed in at least one step in a latter half.

(図 2)



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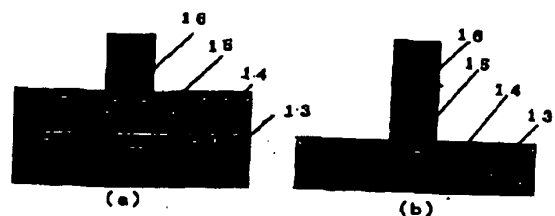
(54) 【発明の名称】 堆積膜表面処理方法

(57) 【要約】 (修正有)

【課題】 プラズマエッチング装置によって処理加工する際に、シリコン堆積膜を、異方性で、高い加工精度によって処理加工することが可能な堆積膜表面処理方法を提供する。

【解決手段】 加工処理をゲート酸化膜14を露出するまでと、ゲート電極多結晶シリコン部15の側壁及びゲート酸化膜14上の残渣を除去するための複数のステップに分けて行うようにし、前半の少なくとも1つのステップにおいて臭化水素 (HBr) ガスまたは臭化水素 (HBr) を含有する混合ガスを用いたプラズマエッチング処理を行い、後半の少なくとも1つのステップにおいて塩素 (Cl₂) と酸素 (O₂) の混合ガスを用いたプラズマエッチング処理を行う。

【図 2】



【特許請求の範囲】

【請求項1】 シリコン堆積膜をプラズマエッチング装置によって処理加工する堆積膜表面処理方法であって、前記加工処理を複数のステップに分けて行うようにし、前記複数のステップの中の前半の少なくとも1つのステップにおいて臭化水素（HBr）ガスまたは臭化水素（HBr）を含有する混合ガスを用いたプラズマエッチング処理を行い、かつ、前記複数のステップの中の後半の少なくとも1つのステップにおいて塩素（Cl₂）と酸素（O₂）の混合ガスを用いてプラズマエッチング処理を行うことを特徴とする堆積膜表面処理方法。

【請求項2】 前記シリコン堆積膜は、導電性の異なる膜を共有するデュアルゲート膜構造のものであることを特徴とする請求項1記載の堆積膜表面処理方法。

【請求項3】 前記シリコン堆積膜は、高融点金属または高融点金属のシリサイドを有するものであることを特徴とする請求項1または2のいずれかに記載の堆積膜表面処理方法。

【請求項4】 前記塩素（Cl₂）と酸素（O₂）の混合ガスは、酸素（O₂）の混合率が0.5%乃至30%の範囲内であることを特徴とする請求項1乃至3のいずれかに記載の堆積膜表面処理方法。

【請求項5】 前記シリコン堆積膜は、加工処理する際に用いるマスクの材料として、炭素を主成分とするもの、窒化シリコンからなるもの、酸化シリコンからなるもの、あるいはこれらを多層にしたものを用いていることを特徴とする請求項1乃至4のいずれかに記載の堆積膜表面処理方法。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、堆積膜表面処理方法に係わり、特に、プラズマ発生装置を用いて半導体素子表面のシリコン堆積膜のエッチング処理を行うのに適した堆積膜表面処理方法に関する。

【0002】

【従来の技術】従来、半導体装置の製造工程においては、半導体素子表面の加工処理、例えば半導体素子の表面に堆積したシリコン堆積膜をエッチング処理する処理工程を含んでいる。そして、このシリコン堆積膜のエッチング処理には、通常、プラズマエッチング装置を用いているもので、エッチング処理すべき半導体素子をプラズマエッチング装置内に入れ、プラズマ雰囲気中で所要のエッチング処理を行っているものである。

【0003】この場合、半導体素子表面のエッチング処理に使用されるプラズマエッチング装置には、主として高い加工精度を得るものとして、米国特許第4,490,209号明細書に開示されたプラズマエッチング装置が知られている。ここに開示されたプラズマエッチング装置は、プラズマとなるガスに臭化水素（HBr）を添加したもので、臭化水素（HBr）を添加したことに

より、被加工物質であるシリコン（Si）膜を異方性にエッチング処理することができるものである。

【0004】ところで、近年、各種の情報内容が高密度化したのに伴い、このような高密度情報を処理する半導体装置の構成も微細構造のものになっており、半導体装置内に形成される大規模集積回路（LSI）についても、配線や電極を加工する際に高い加工精度が要求される。

【0005】このような微細構造の半導体装置において、例えば256Mbitを超えるメモリ素子を構成する場合には、メモリ素子の構成要素となる各MOSトランジスタのゲート酸化膜の厚さを6nm以下に形成する必要がある。そして、このようなMOSトランジスタは、異方性と下地のゲート酸化膜との選択比がトレードオフの関係になるため、エッチング処理によって得ることが極めて難しくなっている。

【0006】これと同時に、近年、半導体装置においては、高速化及び低消費電力化が要望されるに伴い、nMOSトランジスタ等のnMOS素子とpMOSトランジスタ等のpMOS素子とを組み合わせたCMOS素子が多く用いられるようになっている。このCMOS素子は、pMOS側のゲート電極領域となる多結晶シリコン内にp型不純物をドーブし、nMOS側をゲート電極領域となる多結晶シリコン内にn型不純物をドーブしたいわゆるデュアルゲート構造を備えるものである。

【0007】

【発明が解決しようとする課題】CMOS素子のように、導電性を異にするゲート電極、すなわちp型ゲート電極及びn型ゲート電極が混在した相補ゲート電極を備える場合、その相補ゲート電極部分をエッチングによって形成する際には、単一導電性のゲート電極部分をエッチングによって形成する場合に比べて、以下に述べるように、加工上種々の制約が生じることになる。

【0008】すなわち、相補ゲート電極を形成する場合、例えばリソグラフィ工程を増加して、p型ゲート電極領域とn型ゲート電極領域とを個別のエッチング処理によって形成すると、その分処理工程が増えることになり、全体の製造コストが増大するようになる。このため、p型ゲート電極領域とn型ゲート電極領域とは、どうしても同時エッチング処理によって形成する必要がある。これに対し、p型ゲート電極領域とn型ゲート電極領域とを同時エッチング処理によって形成すると、n型ゲート電極となるn型多結晶シリコン部分のエッチング速度が、p型ゲート電極となるp型多結晶シリコン部分のエッチング速度に比べて大きいため、n型ゲート電極領域近傍の下地ゲート酸化膜が早く露出するようになり、露出したゲート酸化膜がエッチング処理され、その処理部分のゲート酸化膜が薄くなったり、その処理部分のゲート酸化膜に突き抜けが生じたりする場合があります。エッチング処理されたn型ゲート電極にサイドエッチが

発生したりする場合もある。

【0009】図3(a)乃至(d)は、n型多結晶シリコン部分を既知の表面処理方法によってプラズマエッチング加工し、n型ゲート電極パターンを得る際に、n型ゲート電極パターンの変化状態を示す断面図であって、

(a)は加工前の状態、(b)乃至(d)は加工後の種々の状態であり、その中で、(b)はゲート酸化膜上にエッチング残渣がある状態、(c)はn型ゲート電極パターンにサイドエッチが入った状態、(d)はゲート酸化膜に突き抜けが生じた状態を示すものである。

【0010】図3(a)乃至(d)において、31はシリコン基板、32はゲート酸化膜、33はn型不純物をドーパしたn型多結晶シリコン部、34はマスク、35はエッチング残渣、36はサイドエッチ、37はゲート酸化膜突き抜け部である。

【0011】まず、プラズマエッチング加工前の状態は、図3(a)に示されるように、シリコン基板31の一面にゲート酸化膜32が形成され、ゲート酸化膜32上にn型多結晶シリコン部33が設けられている。また、n型多結晶シリコン部33上のn型ゲート電極パター

【0012】この場合、既知の表面処理方法においては、プラズマエッチング加工を行う際に、臭化水素(HBr)、塩素(Cl₂)及び酸素(O₂)の混合ガスを用い、エッチング条件として、エッチングトータルガス流量が50乃至300mL/min、処理圧力が0.2乃至4.0Pa、マイクロ波電力が400乃至1000Wで、その混合ガスのガス混合比及び高周波バイアスの電力値をそれぞれ選ぶことにより、好適なプラズマエッチング加工が行われるように設定している。

【0013】しかるに、このようなエッチング条件を設定したとしても、以下に述べるような種々の加工状態になることが多い。

【0014】その第1は、図3(b)に示されるように、ゲート酸化膜32上にエッチング残渣がある加工状態で、マスク34の装着領域に該当するn型ゲート電極パターン(n型多結晶シリコン部33)を除いた大部分のn型多結晶シリコン部33がエッチング除去されているものの、ゲート酸化膜32上に僅かながらエッチング除去されないn型多結晶シリコン部33のエッチング残渣35が残留しているものである。

【0015】その第2は、図3(c)に示されるように、加工されたn型ゲート電極パターンにサイドエッチ36が入った加工状態で、マスク34の装着領域に該当するn型ゲート電極パターン(n型多結晶シリコン部33)を除いた全てのn型多結晶シリコン部33がエッチング除去されているものの、n型ゲート電極パターンの側壁の保護が不十分であるため、ゲート酸化膜32との接合領域に近いn型ゲート電極パターンがエッチング除去され、サイドエッチ36が形成される。

【0016】その第3は、図3(d)に示されるように、ゲート酸化膜32に突き抜け部37が形成された加工状態で、マスク34の装着領域に該当するn型ゲート電極パターン(n型多結晶シリコン部33)を除いた全てのn型多結晶シリコン部33がエッチング除去されているだけでなく、n型ゲート電極パターン周辺のゲート酸化膜32の露出が早かったため、露出したゲート酸化膜32が順次エッチング除去されてしまい、ゲート酸化膜32に突き抜け部37が形成される。

【0017】このように、既知の表面処理方法は、プラズマエッチング加工を行うときのエッチング条件を厳密に設定しない限り、所要の高い加工精度による処理加工を行うことが難しいものであった。

【0018】そこで、ゲート電極パターンのエッチングにおいて、下地のゲート酸化膜が露出した時点で、エッチング時のプロセス、例えば臭化水素(HBr)と塩素(Cl₂)と酸素(O₂)の混合ガスに代えて、臭化水素(HBr)と酸素(O₂)の混合ガスを用いてオーバーエッチングすることにより残渣やサイドエッチやゲート酸化膜の突き抜けを防止する手段が講じられている。この場合、例えば混合ガスの流量を100/5(mL/min)、処理圧力を1.2Pa以上、マイクロ波電力を0.4乃至1.0KW、バイアス電力を30乃至40Wとしてオーバーエッチング処理を実行する。

【0019】しかしながら、この手段は、臭化水素(HBr)と酸素(O₂)の混合ガスによる処理の処理圧力が高く、処理室内へのデポ物の付着が増大するという問題があった。

【0020】本発明は、このような技術的背景に鑑みてなされたもので、その目的は、シリコン堆積膜をプラズマ発生装置によって処理加工する際に、シリコン堆積膜を、異方性で、高い加工精度によって処理加工することを可能にした堆積膜表面処理方法を提供することにある。

【0021】

【課題を解決するための手段】前記目的を達成するために、本発明による堆積膜表面処理方法は、シリコン堆積膜をプラズマエッチング装置によって処理加工するものであって、加工処理を複数のステップに分けて行うようにし、複数のステップの中の前半の少なくとも1つのステップにおいて臭化水素(HBr)ガスまたは臭化水素(HBr)を含有する混合ガスを用いたプラズマエッチング処理を行い、かつ、複数のステップの中の後半の少なくとも1つのステップにおいて塩素(Cl₂)と酸素(O₂)の混合ガスを用いてプラズマエッチング処理を行う手段を具備する。

【0022】前記手段によれば、シリコン堆積膜の下地のゲート酸化膜が露出するまでは、臭化水素(HBr)ガスまたは臭化水素(HBr)を含有する混合ガスを用いた第1のプラズマエッチング処理を行い、この第1の

プラズマエッチング処理によってエッチング残渣がなく、かつ、ゲート酸化膜に突き抜け部が形成されない状態のn型ゲート電極パターンを形成することができ、また、シリコン堆積膜の下地のゲート酸化膜が露出した後は、塩素(Cl₂)と酸素(O₂)の混合ガスを用いた第2のプラズマエッチング処理を行い、この第2のプラズマエッチング処理によって得られた多くの反応生成物がn型ゲート電極パターンの側壁に吸着されるので、n型ゲート電極パターンの側壁が第2のプラズマエッチング処理に対して保護され、サイドエッチが発生しないn型ゲート電極パターンを形成することができる。

【0023】

【発明の実施の形態】以下、本発明の実施の形態を図面を参照して説明する。

【0024】図1は、本発明による堆積膜表面処理方法を実施するのに用いられるプラズマエッチング装置の構成の概要を示す断面図である。

【0025】図1に示されるように、プラズマエッチング装置は、真空容器1と、真空容器1の一端側開口部を封止するマイクロ波導入窓2と、真空容器1の他端側に配置されたガス排気口3と、真空容器1の外周面に沿って設置される電磁石4と、真空容器1の内部に配置され、表面に絶縁膜6が形成された試料台5と、試料台5上に載置された試料となる半導体素子基板7と、一端がマイクロ波導入窓2で終端しているマイクロ波導入部8と、マイクロ波導入部8の他端に接続されたマイクロ波発生源9と、試料台5に導電接続された高周波(RF)バイアス電源10及び可変直流電源11と、真空容器1内にガスを導入するガス導入部12とからなっている。また、真空容器1の内部にプラズマ領域Pが形成される。

【0026】この場合、マイクロ波導入窓2は、材質が石英、セラミック等のマイクロ波(電磁波)の透過物質からなっている。マイクロ波発生源9から出力されたマイクロ波は、マイクロ波導入部8を通り、マイクロ波導入窓2を透過して真空容器1の内部に導入される。ガス導入部12は、ハロゲンガス等のエッチングガスを真空容器1の内部に導入する。真空容器1の内部では、このエッチングガスにマイクロ波が作用し、エッチングガスによるプラズマ領域Pが形成される。電磁石4は、真空容器1内に磁場を発生させるものである。電磁石4が発生する真空容器1内の磁場強度は、真空容器1内に導入されたマイクロ波周波数と共鳴を起すような値に設定されており、例えばマイクロ波周波数が2.45GHzであったとき、磁場強度が0.0875T程度になるように選択される。このような磁場強度に選択されることにより、プラズマ領域P中の電子のサイクロトロン運動がマイクロ波周波数と共鳴し、マイクロ波エネルギーが効率よくプラズマPに供給され、高密度のプラズマPが形成される。

【0027】半導体素子基板7は、シリコン堆積膜がエッチング処理されるもので、試料台5の上に載置される。この試料台5には、表面にセラミックあるいはポリマー膜からなる絶縁膜6が形成されている。高周波バイアス電源10は、試料台5に高周波バイアスを供給し、半導体素子基板7に入射するイオンを加速する。また、可変直流電源11は、直流電圧を試料台5に与え、そのとき発生する静電力によって半導体素子基板7を試料台5の上に保持させるものである。

【0028】ここで、図1に図示のプラズマエッチング装置を用い、半導体素子基板7のシリコン堆積膜をエッチング加工する場合の動作について説明する。この場合、シリコン堆積膜は、多結晶シリコン内にn型不純物をドーブして形成したn型多結晶シリコンであって、このn型多結晶シリコンをエッチング加工し、n型ゲート電極パターンを得るものである。

【0029】図2(a)、(b)は、図1に図示されたプラズマエッチング装置を用い、半導体素子基板7のシリコン堆積膜をプラズマエッチング加工してn型ゲート電極パターンを得る際に、n型ゲート電極パターンの変化状態を示す断面図であって、(a)は加工前の状態、(b)は加工後の状態である。

【0030】図2(a)、(b)において、13はシリコン基板、14はゲート酸化膜、15はn型不純物をドーブしたn型多結晶シリコン部及びn型ゲート電極パターン、16はマスクである。

【0031】そして、プラズマエッチング加工前の状態は、図2(a)に示されるように、シリコン基板13の一面にゲート酸化膜14が形成され、ゲート酸化膜14上にn型多結晶シリコン部15が設けられている。また、n型多結晶シリコン部15上のn型ゲート電極パターン形成部にマスク16が装着されているもので、図3(a)に図示された構成と同じ構成のものである。

【0032】ところで、本発明による堆積膜表面処理方法においては、半導体素子基板7のシリコン堆積膜に対するプラズマエッチング加工を行う際に、複数のステップを経て所要のプラズマエッチング処理を行うもので、プラズマエッチング加工によりゲート酸化膜14が露出するまでの第1のプラズマエッチング処理と、ゲート酸化膜14が露出した後の第2のプラズマエッチング処理とに分かれている。

【0033】この場合、第1のプラズマエッチング処理は、臭化水素(HBr)ガス、または、臭化水素(HBr)を含有する混合ガスを用いたプラズマエッチング処理であって、この場合、臭化水素(HBr)、塩素(Cl₂)及び酸素(O₂)の混合ガスを用い、例えば流量を70/30/3~5(ml/min)、処理圧力を0.2~1.0Pa、マイクロ波電力を0.4~1.0KW、バイアス電力を30Wとし、ゲート酸化膜14の大部分が露出するまでこの第1のプラズマエッチング処

理を実行する。第1のプラズマエッチング処理を行った場合、n型多結晶シリコン部15のマスク16が装着されていない領域は、臭素 (Br)、塩素 (Cl_2) 等のハロゲン原子イオン及びラジカルがn型多結晶シリコン15と反応してエッチング処理が進行し、その処理の結果、n型ゲート電極パターン15が形成される。第1のプラズマエッチング処理時に生成された反応生成物の大部分は排気されるが、反応生成物の一部はn型ゲート電極パターン15の側壁に吸着する。なお、第1のプラズマエッチング処理においては、臭化水素 (HBr) に含まれる水素 (H) 原子がn型ゲート電極パターン15の側壁に吸着する反応生成物の吸着量を抑制する。このため、臭化水素 (HBr) ガスの混合率を高くした場合は、垂直方法のエッチング加工度が向上するものの、n型ゲート電極パターン15にサイドエッチが生じることがあるので、臭化水素 (HBr) ガスの混合率を適宜選択することが好ましい場合がある。

【0034】また、第2のプラズマエッチング処理は、塩素 (Cl_2) 及び酸素 (O_2) の混合ガスを用いたプラズマエッチング処理であって、例えば流量を90/10 (ml/min)、処理圧力を0.3~1.0 Pa、マイクロ波電力を0.4~1.0 KW、バイアス波電力を15 Wとし、ゲート酸化膜14上にエッチング残渣がなくなるまでこの第2のプラズマエッチング処理を実行する。第2のプラズマエッチング処理を行った場合、生成された反応生成物の多くがn型ゲート電極パターン15の側壁に吸着するので、n型ゲート電極パターン15の加工寸法が僅かに大きくなるものの、n型ゲート電極パターン15にサイドエッチが生じることがなく、しかも、エッチング残渣の除去の際に下地のゲート酸化膜14に突き抜け部を形成することがなく、異方性の加工が可能になる。

【0035】その結果、プラズマエッチング加工後の状態は、図2 (b) に示されるように、下地のゲート酸化膜14上にエッチング残渣がなく、n型ゲート電極パターン15にサイドエッチが生じておらず、下地のゲート酸化膜14に突き抜け部も形成されていない状態になり、かつ、異方性の加工が可能となるものである。

【0036】この第2のプラズマエッチング処理に用いる塩素 (Cl_2) 及び酸素 (O_2) の混合ガスは、酸素 (O_2) の混合率が0.5%乃至30%の範囲内に選択することが好ましい。

【0037】一方、マスク16の構成材料は、炭素を主成分とするもの、または、炭素を含まないもののいずれを用いても同じマスク機能を発揮することができるが、窒化シリコンや酸化シリコン等からなる炭素を含まないものを用いた場合、下地のゲート酸化膜14との選択性が高くなる。

【0038】なお、前記の説明においては、本発明による堆積膜表面処理方法でプラズマエッチング処理する半

導体素子基板7のシリコン堆積膜がn型多結晶シリコン部15の単一層である例であったが、本発明による堆積膜表面処理方法の対象となるシリコン堆積膜は、n型多結晶シリコン部15の単一層である例に限られず、堆積膜がp型不純物をドーブしたp型ドーブ領域とn型不純物をドーブしたn型ドーブ領域とを共有するとチューアルゲート膜構造であるもの、シリコン膜上に、タングステン (W)、ニッケル (Ni)、コバルト (Co)、チタン (Ti)、モリブデン (Mo)、クロム (Cr) 等の高融点金属層や、拡散を防ぐバリア膜としてこれらの金属の窒化物を含む層を積層したもの、あるいは、これらの金属のシリサイドを有するシリコン膜であっても、同じようにプラズマエッチング処理を行うことが可能である。

【0039】また、本発明による堆積膜表面処理方法は、プラズマ生成方法に係わりなく、同様の機能を達成させることができる。

【0040】以上の実施の形態によれば、従来行われていた処理圧力の高い臭化水素 (HBr) と酸素 (O_2) の混合ガスによるオーバーエッチング処理に代えて、処理圧力の低い塩素 (Cl_2) と酸素 (O_2) の混合ガスによるオーバーエッチング処理を実行することにより、残渣、サイドエッチ、下地のゲート酸化膜の突き抜けもなく、異方性で高い加工精度のエッチング加工処理ができるとともに、処理室へのデポ物の付着を少なくすることができる。

【0041】

【発明の効果】以上のように、本発明の堆積膜表面処理方法によれば、シリコン堆積膜の下地のゲート酸化膜が露出するまでは、臭化水素 (HBr) ガスまたは臭化水素 (HBr) を含有する混合ガスを用いた第1のプラズマエッチング処理を行い、この第1のプラズマエッチング処理によってエッチング残渣がなく、かつ、ゲート酸化膜に突き抜け部が形成されない状態のn型ゲート電極パターンを形成することができ、また、シリコン堆積膜の下地のゲート酸化膜が露出した後は、塩素 (Cl_2) と酸素 (O_2) の混合ガスを用いた第2のプラズマエッチング処理を行い、この第2のプラズマエッチング処理によって得られた多くの反応生成物がn型ゲート電極パターンの側壁に吸着されるので、n型ゲート電極パターンの側壁が第2のプラズマエッチング処理に対して保護され、サイドエッチが発生しないn型ゲート電極パターンを形成することができるという効果がある。

【図面の簡単な説明】

【図1】本発明による堆積膜表面処理方法を実施するのに用いられるプラズマエッチング装置の構成の概要を示す断面図である。

【図2】図1に図示されたプラズマエッチング装置を用い、半導体素子のシリコン堆積膜をプラズマエッチング加工してn型ゲート電極パターンを得る際に、n型ゲート

ト電極パターンの変化状態を示す断面図である。

【図3】 n型多結晶シリコン部分を既知の表面処理方法によってプラズマエッチング加工し、n型ゲート電極パターンを得る際に、n型ゲート電極パターンの変化状態を示す断面図である。

【符号の説明】

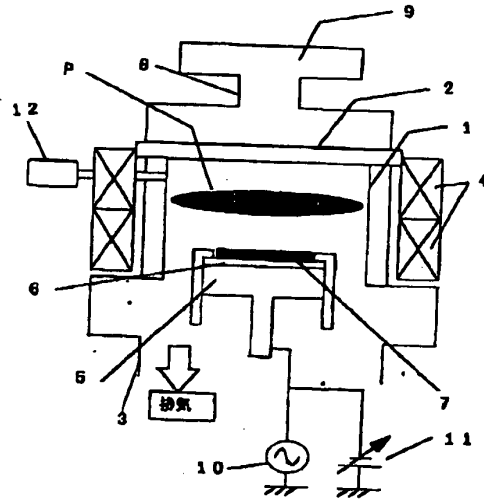
- 1 真空容器
- 2 マイクロ波導入窓
- 3 ガス排気口
- 4 電磁石
- 5 試料台

- 6 絶縁膜
- 7 半導体素子基板(試料)
- 8 マイクロ波導入部
- 9 マイクロ波発生源
- 10 高周波(RF)バイアス電源
- 12 ガス導入部
- 13 シリコン基板
- 14 ゲート酸化膜
- 15 n型多結晶シリコン部(n型ゲート電極パターン)
- 16 マスク

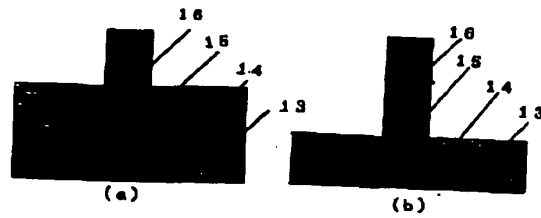
【図1】

【図2】

【図1】

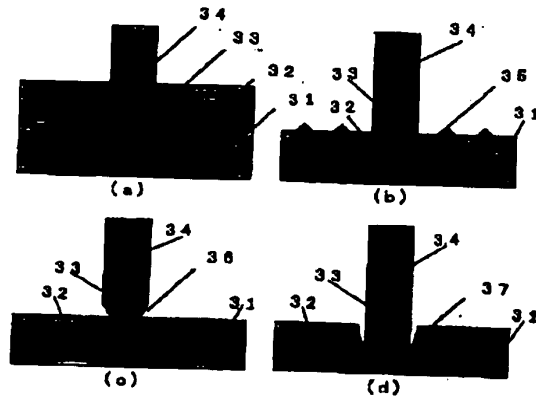


【図2】



【図3】

【図3】



フロントページの続き

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5F033 HH04 HH07 HH15 HH17 HH18
HH19 HH20 HH25 HH26 HH27
HH28 HH29 HH32 HH33 HH34
LL04 MM05 MM07 QQ08 QQ12
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CLAIMS

[Claim(s)]

[Claim 1] It is the deposition film surface treatment approach which carries out processing processing of the silicon deposition film with a plasma etching system. Divide said processing processing into two or more steps, are made to perform it, and plasma-etching processing using the mixed gas which contains hydrogen bromide (HBr) gas or a hydrogen bromide (HBr) in at least one step of the first half in said two or more steps is performed. The deposition film surface treatment approach characterized by performing plasma-etching processing using the mixed gas of chlorine (Cl₂) and oxygen (O₂) in at least one step of the second half in said two or more steps.

[Claim 2] Said silicon deposition film is the deposition film surface treatment approach according to claim 1 characterized by being the thing of JUARU gate membrane structure which shares the film with which conductivity differs.

[Claim 3] Said silicon deposition film is the deposition film surface treatment approach given in either of claims 1 or 2 characterized by being what has the silicide of a refractory metal or a refractory metal.

[Claim 4] The mixed gas of said chlorine (Cl₂) and oxygen (O₂) is the deposition film surface treatment approach according to claim 1 to 3 characterized by being within the limits whose mixing percentage of oxygen (O₂) is 0.5% thru/or 30%.

[Claim 5] Said silicon deposition film is the deposition film surface treatment approach according to claim 1 to 4 characterized by using what uses carbon as a principal component, the thing which consists of silicon nitride, the thing which consists of silicon oxide, or the thing which made these the multilayer as an ingredient of the mask used in case processing processing is carried out.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the deposition film surface treatment approach of having been suitable for performing etching processing of the silicon deposition film on the front face of a semiconductor device especially using a plasma generator, with respect to the deposition film surface treatment approach.

[0002]

[Description of the Prior Art] Conventionally, in the production process of a semiconductor device, down stream processing which carries out etching processing of the silicon deposition film deposited on the processing processing on the front face of a semiconductor device, for example, the front face of a semiconductor device, is included. And usually the plasma etching system is used, the semiconductor device which should carry out etching processing is put in in a plasma etching system, and necessary etching processing is carried out to etching processing of this silicon deposition film in the plasma ambient atmosphere.

[0003] In this case, the plasma etching system indicated by the U.S. Pat. No. 4,490,209 specification is known as what mainly acquires high process tolerance to the plasma etching system used for the etching processing on the front face of a semiconductor device. The plasma etching system indicated here is what added the hydrogen bromide (HBr) in the gas used as the plasma, and can carry out etching processing of the silicon (Si) film which is the quality of a workpiece by having added the hydrogen bromide (HBr) at an anisotropy.

[0004] By the way, the configuration of the semiconductor device which processes such high density information in recent years in connection with various kinds of contents of information having carried out densification is also the thing of the fine structure, and also about the large-scale integrated circuit (LSI) formed in a semiconductor device, in case wiring and an electrode are processed, high process tolerance is required.

[0005] In the semiconductor device of such the fine structure, to constitute the memory device exceeding 256MBit(s), it is necessary to form in 6nm or less the thickness of the gate oxide of each MOS transistor it is thin to the component of a memory device. And since such an MOS transistor becomes the relation of a trade-off of the selection ratio of an anisotropy and the gate oxide of a substrate, obtaining by etching processing is becoming very difficult.

[0006] It can come, simultaneously improvement in the speed and low-power-ization follow on being requested in a semiconductor device in recent years, and many CMOS devices which combined nMOS components, such as a nMOS transistor, and pMOS components, such as a pMOS transistor, are used. This CMOS device dopes p mold impurity in the polycrystalline silicon used as the gate electrode field by the side of pMOS, and is equipped with the so-called JUARU gate structure which doped n mold impurity in the polycrystalline silicon which serves as a gate electrode field in the nMOS side.

[0007]

[Problem(s) to be Solved by the Invention] when it has the complementary gate electrode with which the

gate electrode which differs in conductivity, i.e., p mold gate electrode, and n mold gate electrode were intermingled like a CMOS device, in case the complementary gate electrode section is formed by etching, constraint of processing top versatility will arise so that a single conductive gate electrode section may be described below compared with the case where 4s ** are formed in etching.

[0008] That is, if a lithography process is increased and p mold gate electrode field and n mold gate electrode field are formed by etching processing according to individual when forming a complementary gate electrode for example, the part down stream processing will increase and the whole manufacturing cost will come to increase. For this reason, it is surely necessary to form p mold gate electrode field and n mold gate electrode field by coincidence etching processing. On the other hand, if p mold gate electrode field and n mold gate electrode field are formed by coincidence etching processing It compares with the etch rate of p mold polycrystalline silicon part from which the etch rate of n mold polycrystalline silicon part used as n mold gate electrode serves as p mold gate electrode. Since it is large, The substrate gate oxide near the n mold gate electrode field comes to be early exposed. Etching processing of the exposed gate oxide is carried out, the gate oxide of the processing part may become thin, or it may poke to the gate oxide of the processing part, an omission may arise, and side etch may occur in n mold gate electrode by which etching processing was carried out.

[0009] Drawing 3 (a) thru/or (d) carry out plasma-etching processing of the n mold polycrystalline silicon part by the known surface-preparation approach. In case n mold gate electrode pattern is obtained, it is the sectional view showing the change condition of n mold gate electrode pattern, and the condition before processing, (b), or (d) of (a) is in the various conditions after processing. In it The condition that (b) has an etch residue on gate oxide, and (c) show the condition that poked the condition containing side etch, and (d) to n mold gate electrode pattern at gate oxide, and the omission arose.

[0010] For n mold polycrystalline silicon section in which a silicon substrate and 32 doped gate oxide and, as for 33, 31 doped n mold impurity, and 34, as for an etch residue and 36, in drawing 3 (a) thru/or (d), a mask and 35 are [side etch and 37] the gate oxide thrust omission sections.

[0011] First, as the condition before plasma-etching processing is shown in drawing 3 (a), gate oxide 32 is formed in the whole surface of a silicon substrate 31, and n mold polycrystalline silicon section 33 is formed on gate oxide 32. Moreover, n mold gate electrode pattern formation section on n mold polycrystalline silicon section 33 is equipped with the mask 34.

[0012] In the known surface-preparation approach, in case plasma-etching processing is performed, the mixed gas of a hydrogen bromide (HBr), chlorine (Cl₂), and oxygen (O₂) is used. In this case, as etching conditions 0.2 thru/or 4.0Pa, and microwave power by 400 thru/or 1000W [an etching total quantity of gas flow] [50 thru/or 300 mL/min, and the processing pressure force] By choosing the gas mixture ratio of the mixed gas, and the power value of high frequency bias, respectively, it has set up so that suitable plasma-etching processing may be performed.

[0013] However, even if it sets up such etching conditions, it will be in various processing conditions which are described below in many cases.

[0014] As the 1st is shown in the drawing 3 (b), although etching removal of the n mold polycrystalline silicon section 33 of most except n mold gate electrode pattern (n mold polycrystalline silicon section 33) which is in the processing condition which has an etch residue on gate oxide 32, and corresponds to the wearing field of a mask 34 is carried out, the etch residue 35 of n mold polycrystalline silicon section 33 by which etching removal is not slightly carried out on gate oxide 32 remains.

[0015] The 2nd is in the processing condition in which side etch 36 went into processed n mold gate electrode pattern, as shown in the drawing 3 (c). Although etching removal of all the n mold polycrystalline silicon sections 33 except n mold gate electrode pattern (n mold polycrystalline silicon section 33) applicable to the wearing field of a mask 34 is carried out Since protection of the side attachment wall of n mold gate electrode pattern is inadequate, etching removal of the n mold gate electrode pattern near a junction field with gate oxide 32 is carried out, and side etch 36 is formed.

[0016] The 3rd is in the processing condition that ran in gate oxide 32 and the section 37 was formed, as shown in the drawing 3 (d). Etching removal of all the n mold polycrystalline silicon sections 33 except n mold gate electrode pattern (n mold polycrystalline silicon section 33) applicable to the wearing field

of a mask 34 is not only carried out, but Since exposure of the gate oxide 32 of n mold gate electrode pattern circumference was early, sequential etching removal of the exposed gate oxide 32 will be carried out, it runs in gate oxide 32, and the section 37 is formed.

[0017] Thus, unless the etching conditions when performing plasma-etching processing were set up strictly, it was difficult for the known surface-preparation approach to perform processing processing by necessary high process tolerance.

[0018] Then, in etching of a gate electrode pattern, when the gate oxide of a substrate is exposed, it replaces with the process at the time of etching, for example, the mixed gas of a hydrogen bromide (HBr), chlorine (Cl₂), and oxygen (O₂), and a means to prevent the thrust omission of residue, side etch, or gate oxide is provided by carrying out over etching using the mixed gas of a hydrogen bromide (HBr) and oxygen (O₂). Over etching processing is performed using [the flow rate of mixed gas] 0.4 thru/or 1.0kW, and bias power as 30 thru/or 40W for microwave power in this case using 100/5 (ml/min) and the processing pressure force as 1.2Pa or more.

[0019] However, this means had the problem that the processing pressure force of processing by the mixed gas of a hydrogen bromide (HBr) and oxygen (O₂) was high, and adhesion of the depository object to the processing interior of a room increased.

[0020] In case this invention was made in view of such a technological background and the purpose carries out processing processing of the silicon deposition film with a plasma generator, it is in offering the deposition film surface treatment approach which made it possible to be an anisotropy and to carry out processing processing of the silicon deposition film with high process tolerance.

[0021]

[Means for Solving the Problem] In order to attain said purpose, the deposition film surface treatment approach by this invention It is what carries out processing processing of the silicon deposition film with a plasma etching system. Divide processing processing into two or more steps, are made to perform it, and plasma-etching processing using the mixed gas which contains hydrogen bromide (HBr) gas or a hydrogen bromide (HBr) in at least one step of the first half in two or more steps is performed. A means to perform plasma-etching processing using the mixed gas of chlorine (Cl₂) and oxygen (O₂) in at least one step of the second half in two or more steps is provided.

[0022] Until the gate oxide of the substrate of the silicon deposition film is exposed according to said means 1st [using the mixed gas containing hydrogen bromide (HBr) gas or a hydrogen bromide (HBr)] plasma-etching processing is performed. There is no etch residue by this 1st plasma-etching processing. And after it can form n mold gate electrode pattern in the condition that run in gate oxide and the section is not formed and the gate oxide of the substrate of the silicon deposition film is exposed Since the side attachment wall of n mold gate electrode pattern is adsorbed, many resultants which performed 2nd [using the mixed gas of chlorine (Cl₂) and oxygen (O₂)] plasma-etching processing, and were acquired by this 2nd plasma-etching processing The side attachment wall of n mold gate electrode pattern is protected to the 2nd plasma-etching processing, and n mold gate electrode pattern which side etch does not generate can be formed.

[0023]

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained with reference to a drawing.

[0024] Drawing 1 is the sectional view showing the outline of the configuration of the plasma etching system used for enforcing the deposition film surface-preparation approach by this invention.

[0025] As shown in drawing 1, a plasma etching system A vacuum housing 1 and the microwave installation aperture 2 which closes end side opening of a vacuum housing 1, The flueing opening 3 arranged at the other end side of a vacuum housing 1, and the electromagnet 4 installed along with the peripheral face of a vacuum housing 1, The sample base 5 where it has been arranged inside a vacuum housing 1, and the insulator layer 6 was formed in the front face, The semiconductor device substrate 7 used as the sample laid on the sample base 5, and the microwave induction 8 in which the end is carrying out termination by the microwave installation aperture 2, It consists of the microwave generation source 9 connected to the other end of the microwave induction 8, the high frequency (RF)

bias power supply 10 and adjustable DC power supply 11 which were connected conductively to the sample base 5, and gas induction 12 to which gas is introduced in a vacuum housing 1. Moreover, the plasma field P is formed in the interior of a vacuum housing 1.

[0026] In this case, as for the microwave installation aperture 2, the quality of the material consists of transparency matter of microwave (electromagnetic wave), such as a quartz and a ceramic. The microwave outputted from the microwave generation source 9 passes along the microwave induction 8, penetrates the microwave installation aperture 2, and is introduced into the interior of a vacuum housing 1. The gas induction 12 introduces etching gas, such as halogen gas, into the interior of a vacuum housing 1. Inside a vacuum housing 1, microwave acts on this etching gas and the plasma field P by etching gas is formed. An electromagnet 4 generates a magnetic field in a vacuum housing 1. The magnetic field strength in the vacuum housing 1 which an electromagnet 4 generates is chosen so that it is set as the microwave frequency introduced in the vacuum housing 1, and a value which causes resonance, for example, magnetic field strength may turn into about 0.0875T, when a microwave frequency is 2.45GHz. By being chosen as such magnetic field strength, cyclotron movement of the electron in the plasma field P resonates with a microwave frequency; microwave energy is efficiently supplied to Plasma P, and the plasma P of high density is formed.

[0027] Etching processing of the silicon deposition film is carried out, and the semiconductor device substrate 7 is laid on the sample base 5. In this sample base 5, the insulator layer 6 which consists of a ceramic or polymer film is formed in the front face. The high frequency bias power supply 10 supplies high frequency bias to the sample base 5, and the ion which carries out incidence to the semiconductor device substrate 7 is accelerated. Moreover, adjustable DC power supply 11 give direct current voltage to the sample base 5, and make the semiconductor device substrate 7 hold on the sample base 5 according to the electrostatic force then generated.

[0028] Here, the actuation in the case of carrying out etching processing of the silicon deposition film of the semiconductor device substrate 7 is explained to drawing 1 using the plasma etching system of illustration. In this case, the silicon deposition film is n mold polycrystalline silicon which doped and formed n mold impurity in polycrystalline silicon, carries out etching processing of this n mold polycrystalline silicon, and obtains n mold gate electrode pattern.

[0029] In case drawing 2 (a) and (b) carry out plasma-etching processing of the silicon deposition film of the semiconductor device substrate 7 using the plasma etching system illustrated by drawing 1 and n mold gate electrode pattern is obtained, it is the sectional view showing the change condition of n mold gate electrode pattern, and (a) is in the condition before processing and (b) is in the condition after processing.

[0030] In drawing 2 (a) and (b), n mold polycrystalline silicon section and n mold gate electrode pattern with which a silicon substrate and 14 doped gate oxide and, as for 15, 13 doped n mold impurity, and 16 are masks.

[0031] And as the condition before plasma-etching processing is shown in drawing 2 (a), gate oxide 14 is formed in the whole surface of a silicon substrate 13, and n mold polycrystalline silicon section 15 is formed on gate oxide 14. Moreover, it is the thing of the same configuration as the configuration which n mold gate electrode pattern formation section on n mold polycrystalline silicon section 15 is equipped with the mask 16, and was illustrated by drawing 3 (a).

[0032] By the way, in the deposition film surface-preparation approach by this invention, in case plasma-etching processing to the silicon deposition film of the semiconductor device substrate 7 is performed, necessary plasma-etching processing is performed through two or more steps, and it is divided into the 1st plasma-etching processing until gate oxide 14 is exposed with plasma-etching processing, and the 2nd plasma-etching processing after gate oxide 14 is exposed.

[0033] The 1st plasma-etching processing In this case, hydrogen bromide (HBr) gas, Or it is plasma-etching processing using the mixed gas containing a hydrogen bromide (HBr). In this case, the mixed gas of a hydrogen bromide (HBr), chlorine (Cl₂), and oxygen (O₂) is used. For example, this 1st plasma-etching processing is performed until it sets 0.2-1.0Pa and microwave power to 0.4-1.0kW, it sets bias power to 30W for 70/30/3-5 (ml/min) and the processing pressure force and the great portion of

gate oxide 14 exposes a flow rate. When 1st plasma-etching processing is performed, halogen atom ion and radicals, such as a bromine (Br) and chlorine (Cl₂), react with n mold polycrystalline silicon 15, etching processing advances, and, as for the field where it is not equipped with the mask 16 of n mold polycrystalline silicon section 15, n mold gate electrode pattern 15 is formed as a result of the processing. Although most resultants generated at the time of the 1st plasma-etching processing are exhausted, some resultants stick to the side attachment wall of n mold gate electrode pattern 15. In addition, in the 1st plasma-etching processing, the amount of adsorption of the resultant with which the hydrogen (H₂) atom contained in a hydrogen bromide (HBr) sticks to the side attachment wall of n mold gate electrode pattern 15 is controlled. For this reason, since side etch may arise to n mold gate electrode pattern 15 although the etching workability of the perpendicular approach improves when mixing percentage of hydrogen bromide (HBr) gas is made high, it may be desirable to choose the mixing percentage of hydrogen bromide (HBr) gas suitably.

[0034] Moreover, the 2nd plasma-etching processing is the plasma-etching processing which used the mixed gas of chlorine (Cl₂) and oxygen (O₂), for example, it performs this 2nd plasma-etching processing until it sets 90/10 (ml/min) and the processing pressure force to 0.3-1.0Pa, it sets 0.4-1.0kW and bias wave power to 15W for microwave power and an etch residue is lost on gate oxide 14 in a flow rate. Since many of generated resultants stick to the side attachment wall of n mold gate electrode pattern 15 when 2nd plasma-etching processing is performed, although the processing dimension of n mold gate electrode pattern 15 becomes large slightly, side etch does not arise to n mold gate electrode pattern 15, moreover, it runs in the gate oxide 14 of a substrate, the section is not formed in the case of removal of an etch residue, and processing of an anisotropy is attained.

[0035] Consequently, as shown in drawing 2 (b), side etch does not arise to n mold gate electrode pattern 15, but it runs through the condition after plasma-etching processing in the gate oxide 14 of a substrate, and it will be [there is no etch residue on the gate oxide 14 of a substrate,] in the condition that the section is not formed, either, and will become processible [an anisotropy].

[0036] As for the mixed gas of the chlorine (Cl₂) used for this 2nd plasma-etching processing, and oxygen (O₂), it is desirable to choose it as within the limits whose mixing percentage of oxygen (O₂) is 0.5% thru/or 30%.

[0037] On the other hand, although the component of a mask 16 does not contain the thing which uses carbon as a principal component, or carbon, even if it uses any, the same mask function can be demonstrated, but when what does not contain the carbon which consists of silicon nitride, silicon oxide, etc. is used, selectivity with the gate oxide 14 of a substrate becomes high.

[0038] In addition, although the silicon deposition film of the semiconductor device substrate 7 which carries out plasma-etching processing by the deposition film surface-preparation approach by this invention was the example which is the monolayer of n mold polycrystalline silicon section 15 in the aforementioned explanation The silicon deposition film set as the object of the deposition film surface treatment approach by this invention What is JUARU gate membrane structure when p mold dope field where it was not restricted to the example which is the monolayer of n mold polycrystalline silicon section 15, but the deposition film doped p mold impurity, and n mold dope field which doped n mold impurity are shared, On the silicon film, a tungsten (W), nickel (nickel), cobalt (Co), What carried out the laminating of refractory metal layers, such as titanium (Ti), molybdenum (Mo), and chromium (Cr), and the layer which contains the nitride of these metals as barrier film which prevents diffusion, Or even if it is the silicon film which has the silicide of these metals, it is possible to perform plasma-etching processing similarly.

[0039] Moreover, there is no deposition film surface treatment approach by this invention, and it can make the same function attain with respect to the plasma production approach.

[0040] According to the gestalt of the above operation, it replaces with the over etching processing by the mixed gas of the high hydrogen bromide (HBr) and oxygen (O₂) of the processing pressure force currently performed conventionally. By performing over etching processing by the mixed gas of the low chlorine (Cl₂) of the processing pressure force, and oxygen (O₂) the gate oxide of residue, side etch, and a substrate -- also running -- while there is nothing and being able to perform etching processing

processing of high process tolerance in an anisotropy, adhesion of the depository object to a processing room can be lessened.

[0041]

[Effect of the Invention] As mentioned above, until the gate oxide of the substrate of the silicon deposition film is exposed according to the deposition film surface treatment approach of this invention 1st [using the mixed gas containing hydrogen bromide (HBr) gas or a hydrogen bromide (HBr)] plasma-etching processing is performed. There is no etch residue by this 1st plasma-etching processing. And after it can form n mold gate electrode pattern in the condition that run in gate oxide and the section is not formed and the gate oxide of the substrate of the silicon deposition film is exposed Since the side attachment wall of n mold gate electrode pattern is adsorbed, many resultants which performed 2nd [using the mixed gas of chlorine (Cl₂) and oxygen (O₂)] plasma-etching processing, and were acquired by this 2nd plasma-etching processing The side attachment wall of n mold gate electrode pattern is protected to the 2nd plasma-etching processing, and it is effective in the ability to form n mold gate electrode pattern which side etch does not generate.

[Translation done.]

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TECHNICAL FIELD

[Field of the Invention] This invention relates to the deposition film surface treatment approach of having been suitable for performing etching processing of the silicon deposition film on the front face of a semiconductor device especially using a plasma generator, with respect to the deposition film surface treatment approach.

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PRIOR ART

[Description of the Prior Art] Conventionally, in the production process of a semiconductor device, down stream processing which carries out etching processing of the silicon deposition film deposited on the processing processing on the front face of a semiconductor device, for example, the front face of a semiconductor device, is included. And usually the plasma etching system is used, the semiconductor device which should carry out etching processing is put in in a plasma etching system, and necessary etching processing is carried out to etching processing of this silicon deposition film in the plasma ambient atmosphere.

[0003] In this case, the plasma etching system indicated by the U.S. Pat. No. 4,490,209 specification is known as what mainly acquires high process tolerance to the plasma etching system used for the etching processing on the front face of a semiconductor device. The plasma etching system indicated here is what added the hydrogen bromide (HBr) in the gas used as the plasma, and can carry out etching processing of the silicon (Si) film which is the quality of a workpiece by having added the hydrogen bromide (HBr) at an anisotropy.

[0004] By the way, the configuration of the semiconductor device which processes such high density information in recent years in connection with various kinds of contents of information having carried out densification is also the thing of the fine structure, and also about the large-scale integrated circuit (LSI) formed in a semiconductor device, in case wiring and an electrode are processed, high process tolerance is required.

[0005] In the semiconductor device of such the fine structure, to constitute the memory device exceeding 256MBit(s), it is necessary to form in 6nm or less the thickness of the gate oxide of each MOS transistor it is thin to the component of a memory device. And since such an MOS transistor becomes the relation of a trade-off of the selection ratio of an anisotropy and the gate oxide of a substrate, obtaining by etching processing is becoming very difficult.

[0006] It can come, simultaneously improvement in the speed and low-power-ization follow on being requested in a semiconductor device in recent years, and many CMOS devices which combined nMOS components, such as a nMOS transistor, and pMOS components, such as a pMOS transistor, are used. This CMOS device dopes p mold impurity in the polycrystalline silicon used as the gate electrode field by the side of pMOS, and is equipped with the so-called JUARU gate structure which doped n mold impurity in the polycrystalline silicon which serves as a gate electrode field in the nMOS side.

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EFFECT OF THE INVENTION

[Effect of the Invention] As mentioned above, until the gate oxide of the substrate of the silicon deposition film is exposed according to the deposition film surface treatment approach of this invention 1st [using the mixed gas containing hydrogen bromide (HBr) gas or a hydrogen bromide (HBr)] plasma-etching processing is performed. There is no etch residue by this 1st plasma-etching processing. And after it can form n mold gate electrode pattern in the condition that run in gate oxide and the section is not formed and the gate oxide of the substrate of the silicon deposition film is exposed Since the side attachment wall of n mold gate electrode pattern is adsorbed, many resultants which performed 2nd [using the mixed gas of chlorine (Cl₂) and oxygen (O₂)] plasma-etching processing, and were acquired by this 2nd plasma-etching processing The side attachment wall of n mold gate electrode pattern is protected to the 2nd plasma-etching processing, and it is effective in the ability to form n mold gate electrode pattern which side etch does not generate.

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 TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] when it has the complementary gate electrode with which the gate electrode which differs in conductivity, i.e., p mold gate electrode, and n mold gate electrode were intermingled like a CMOS device, in case the complementary gate electrode section is formed by etching, constraint of processing top versatility will arise so that a single conductive gate electrode section may be described below compared with the case where 4s ** are formed in etching.

[0008] That is, if a lithography process is increased and p mold gate electrode field and n mold gate electrode field are formed by etching processing according to individual when forming a complementary gate electrode for example, the part down stream processing will increase and the whole manufacturing cost will come to increase. For this reason, it is surely necessary to form p mold gate electrode field and n mold gate electrode field by coincidence etching processing. On the other hand, if p mold gate electrode field and n mold gate electrode field are formed by coincidence etching processing It compares with the etch rate of p mold polycrystalline silicon part from which the etch rate of n mold polycrystalline silicon part used as n mold gate electrode serves as p mold gate electrode. Since it is large, The substrate gate oxide near the n mold gate electrode field comes to be early exposed. Etching processing of the exposed gate oxide is carried out, the gate oxide of the processing part may become thin, or it may poke to the gate oxide of the processing part, an omission may arise, and side etch may occur in n mold gate electrode by which etching processing was carried out.

[0009] Drawing 3 (a) thru/or (d) carry out plasma-etching processing of the n mold polycrystalline silicon part by the known surface-preparation approach. In case n mold gate electrode pattern is obtained, it is the sectional view showing the change condition of n mold gate electrode pattern, and the condition before processing, (b), or (d) of (a) is in the various conditions after processing. In it The condition that (b) has an etch residue on gate oxide, and (c) show the condition that poked the condition containing side etch, and (d) to n mold gate electrode pattern at gate oxide, and the omission arose.

[0010] For n mold polycrystalline silicon section in which a silicon substrate and 32 doped gate oxide and, as for 33, 31 doped n mold impurity, and 34, as for an etch residue and 36, in drawing 3 (a) thru/or (d), a mask and 35 are [side etch and 37] the gate oxide thrust omission sections.

[0011] First, as the condition before plasma-etching processing is shown in drawing 3 (a), gate oxide 32 is formed in the whole surface of a silicon substrate 31, and n mold polycrystalline silicon section 33 is formed on gate oxide 32. Moreover, n mold gate electrode pattern formation section on n mold polycrystalline silicon section 33 is equipped with the mask 34.

[0012] In the known surface-preparation approach, in case plasma-etching processing is performed, the mixed gas of a hydrogen bromide (HBr), chlorine (Cl₂), and oxygen (O₂) is used. In this case, as etching conditions 0.2 thru/or 4.0Pa, and microwave power by 400 thru/or 1000W [an etching total quantity of gas flow] [50 thru/or 300 mL/min, and the processing pressure force] By choosing the gas mixture ratio of the mixed gas, and the power value of high frequency bias, respectively, it has set up so that suitable plasma-etching processing may be performed.

[0013] However, even if it sets up such etching conditions, it will be in various processing conditions which are described below in many cases.

[0014] As the 1st is shown in the drawing 3 (b), although etching removal of the n mold polycrystalline silicon section 33 of most except n mold gate electrode pattern (n mold polycrystalline silicon section 33) which is in the processing condition which has an etch residue on gate oxide 32, and corresponds to the wearing field of a mask 34 is carried out, the etch residue 35 of n mold polycrystalline silicon section 33 by which etching removal is not slightly carried out on gate oxide 32 remains.

[0015] The 2nd is in the processing condition in which side etch 36 went into processed n mold gate electrode pattern, as shown in the drawing 3 (c). Although etching removal of all the n mold polycrystalline silicon sections 33 except n mold gate electrode pattern (n mold polycrystalline silicon section 33) applicable to the wearing field of a mask 34 is carried out Since protection of the side attachment wall of n mold gate electrode pattern is inadequate, etching removal of the n mold gate electrode pattern near a junction field with gate oxide 32 is carried out, and side etch 36 is formed.

[0016] The 3rd is in the processing condition that ran in gate oxide 32 and the section 37 was formed, as shown in the drawing 3 (d). Etching removal of all the n mold polycrystalline silicon sections 33 except n mold gate electrode pattern (n mold polycrystalline silicon section 33) applicable to the wearing field of a mask 34 is not only carried out, but Since exposure of the gate oxide 32 of n mold gate electrode pattern circumference was early, sequential etching removal of the exposed gate oxide 32 will be carried out, it runs in gate oxide 32, and the section 37 is formed.

[0017] Thus, unless the etching conditions when performing plasma-etching processing were set up strictly, it was difficult for the known surface-preparation approach to perform processing processing by necessary high process tolerance.

[0018] Then, in etching of a gate electrode pattern, when the gate oxide of a substrate is exposed, it replaces with the process at the time of etching, for example, the mixed gas of a hydrogen bromide (HBr), chlorine (Cl₂), and oxygen (O₂), and a means to prevent the thrust omission of residue, side etch, or gate oxide is provided by carrying out over etching using the mixed gas of a hydrogen bromide (HBr) and oxygen (O₂). Over etching processing is performed using [the flow rate of mixed gas] 0.4 thru/or 1.0kW, and bias power as 30 thru/or 40W for microwave power in this case using 100/5 (ml/min) and the processing pressure force as 1.2Pa or more.

[0019] However, this means had the problem that the processing pressure force of processing by the mixed gas of a hydrogen bromide (HBr) and oxygen (O₂) was high, and adhesion of the depository object to the processing interior of a room increased.

[0020] In case this invention was made in view of such a technological background and the purpose carries out processing processing of the silicon deposition film with a plasma generator, it is in offering the deposition film surface treatment approach which made it possible to be an anisotropy and to carry out processing processing of the silicon deposition film with high process tolerance.

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MEANS

[Means for Solving the Problem] In order to attain said purpose, the deposition film surface treatment approach by this invention It is what carries out processing processing of the silicon deposition film with a plasma etching system. Divide processing processing into two or more steps, are made to perform it, and plasma-etching processing using the mixed gas which contains hydrogen bromide (HBr) gas or a hydrogen bromide (HBr) in at least one step of the first half in two or more steps is performed. A means to perform plasma-etching processing using the mixed gas of chlorine (Cl₂) and oxygen (O₂) in at least one step of the second half in two or more steps is provided.

[0022] Until the gate oxide of the substrate of the silicon deposition film is exposed according to said means 1st [using the mixed gas containing hydrogen bromide (HBr) gas or a hydrogen bromide (HBr)] plasma-etching processing is performed. There is no etch residue by this 1st plasma-etching processing. And after it can form n mold gate electrode pattern in the condition that run in gate oxide and the section is not formed and the gate oxide of the substrate of the silicon deposition film is exposed Since the side attachment wall of n mold gate electrode pattern is adsorbed, many resultants which performed 2nd [using the mixed gas of chlorine (Cl₂) and oxygen (O₂)] plasma-etching processing, and were acquired by this 2nd plasma-etching processing The side attachment wall of n mold gate electrode pattern is protected to the 2nd plasma-etching processing, and n mold gate electrode pattern which side etch does not generate can be formed.

[0023]

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained with reference to a drawing.

[0024] Drawing 1 is the sectional view showing the outline of the configuration of the plasma etching system used for enforcing the deposition film surface-preparation approach by this invention.

[0025] As shown in drawing 1 , a plasma etching system A vacuum housing 1 and the microwave installation aperture 2 which closes end side opening of a vacuum housing 1, The flueing opening 3 arranged at the other end side of a vacuum housing 1, and the electromagnet 4 installed along with the peripheral face of a vacuum housing 1, The sample base 5 where it has been arranged inside a vacuum housing 1, and the insulator layer 6 was formed in the front face, The semiconductor device substrate 7 used as the sample laid on the sample base 5, and the microwave induction 8 in which the end is carrying out termination by the microwave installation aperture 2, It consists of the microwave generation source 9 connected to the other end of the microwave induction 8, the high frequency (RF) bias power supply 10 and adjustable DC power supply 11 which were connected conductively to the sample base 5, and gas induction 12 to which gas is introduced in a vacuum housing 1. Moreover, the plasma field P is formed in the interior of a vacuum housing 1.

[0026] In this case, as for the microwave installation aperture 2, the quality of the material consists of transparency matter of microwave (electromagnetic wave), such as a quartz and a ceramic. The microwave outputted from the microwave generation source 9 passes along the microwave induction 8, penetrates the microwave installation aperture 2, and is introduced into the interior of a vacuum housing 1. The gas induction 12 introduces etching gas, such as halogen gas, into the interior of a vacuum

housing 1. Inside a vacuum housing 1, microwave acts on this etching gas and the plasma field P by etching gas is formed. An electromagnet 4 generates a magnetic field in a vacuum housing 1. The magnetic field strength in the vacuum housing 1 which an electromagnet 4 generates is chosen so that it is set as the microwave frequency introduced in the vacuum housing 1, and a value which causes resonance, for example, magnetic field strength may turn into about 0.0875T, when a microwave frequency is 2.45GHz. By being chosen as such magnetic field strength, cyclotron movement of the electron in the plasma field P resonates with a microwave frequency, microwave energy is efficiently supplied to Plasma P, and the plasma P of high density is formed.

[0027] Etching processing of the silicon deposition film is carried out, and the semiconductor device substrate 7 is laid on the sample base 5. In this sample base 5, the insulator layer 6 which consists of a ceramic or polymer film is formed in the front face. The high frequency bias power supply 10 supplies high frequency bias to the sample base 5, and the ion which carries out incidence to the semiconductor device substrate 7 is accelerated. Moreover, adjustable DC power supply 11 give direct current voltage to the sample base 5, and make the semiconductor device substrate 7 hold on the sample base 5 according to the electrostatic force then generated.

[0028] Here, the actuation in the case of carrying out etching processing of the silicon deposition film of the semiconductor device substrate 7 is explained to drawing 1 using the plasma etching system of illustration. In this case, the silicon deposition film is n mold polycrystalline silicon which doped and formed n mold impurity in polycrystalline silicon, carries out etching processing of this n mold polycrystalline silicon, and obtains n mold gate electrode pattern.

[0029] In case drawing 2 (a) and (b) carry out plasma-etching processing of the silicon deposition film of the semiconductor device substrate 7 using the plasma etching system illustrated by drawing 1 and n mold gate electrode pattern is obtained, it is the sectional view showing the change condition of n mold gate electrode pattern, and (a) is in the condition before processing and (b) is in the condition after processing.

[0030] In drawing 2 (a) and (b), n mold polycrystalline silicon section and n mold gate electrode pattern with which a silicon substrate and 14 doped gate oxide and, as for 15, 13 doped n mold impurity, and 16 are masks.

[0031] And as the condition before plasma-etching processing is shown in drawing 2 (a), gate oxide 14 is formed in the whole surface of a silicon substrate 13, and n mold polycrystalline silicon section 15 is formed on gate oxide 14. Moreover, it is the thing of the same configuration as the configuration which n mold gate electrode pattern formation section on n mold polycrystalline silicon section 15 is equipped with the mask 16, and was illustrated by drawing 3 (a).

[0032] By the way, in the deposition film surface-preparation approach by this invention, in case plasma-etching processing to the silicon deposition film of the semiconductor device substrate 7 is performed, necessary plasma-etching processing is performed through two or more steps, and it is divided into the 1st plasma-etching processing until gate oxide 14 is exposed with plasma-etching processing, and the 2nd plasma-etching processing after gate oxide 14 is exposed.

[0033] The 1st plasma-etching processing In this case, hydrogen bromide (HBr) gas, Or it is plasma-etching processing using the mixed gas containing a hydrogen bromide (HBr). In this case, the mixed gas of a hydrogen bromide (HBr), chlorine (Cl₂), and oxygen (O₂) is used. For example, this 1st plasma-etching processing is performed until it sets 0.2-1.0Pa and microwave power to 0.4-1.0kW, it sets bias power to 30W for 70/30/3-5 (ml/min) and the processing pressure force and the great portion of gate oxide 14 exposes a flow rate. When 1st plasma-etching processing is performed, halogen atom ion and radicals, such as a bromine (Br) and chlorine (Cl₂), react with n mold polycrystalline silicon 15, etching processing advances, and, as for the field where it is not equipped with the mask 16 of n mold polycrystalline silicon section 15, n mold gate electrode pattern 15 is formed as a result of the processing. Although most resultants generated at the time of the 1st plasma-etching processing are exhausted, some resultants stick to the side attachment wall of n mold gate electrode pattern 15. In addition, in the 1st plasma-etching processing, the amount of adsorption of the resultant with which the hydrogen (H₂) atom contained in a hydrogen bromide (HBr) sticks to the side attachment wall of n mold

gate electrode pattern 15 is controlled. For this reason, since side etch may arise to n mold gate electrode pattern 15 although the etching workability of the perpendicular approach improves when mixing percentage of hydrogen bromide (HBr) gas is made high, it may be desirable to choose the mixing percentage of hydrogen bromide (HBr) gas suitably.

[0034] Moreover, the 2nd plasma-etching processing is the plasma-etching processing which used the mixed gas of chlorine (Cl₂) and oxygen (O₂), for example, it performs this 2nd plasma-etching processing until it sets 90/10 (ml/min) and the processing pressure force to 0.3-1.0Pa, it sets 0.4-1.0kW and bias wave power to 15W for microwave power and an etch residue is lost on gate oxide 14 in a flow rate. Since many of generated resultants stick to the side attachment wall of n mold gate electrode pattern 15 when 2nd plasma-etching processing is performed, although the processing dimension of n mold gate electrode pattern 15 becomes large slightly, side etch does not arise to n mold gate electrode pattern 15, moreover, it runs in the gate oxide 14 of a substrate, the section is not formed in the case of removal of an etch residue, and processing of an anisotropy is attained.

[0035] Consequently, as shown in drawing 2 (b), side etch does not arise to n mold gate electrode pattern 15, but it runs through the condition after plasma-etching processing in the gate oxide 14 of a substrate, and it will be [there is no etch residue on the gate oxide 14 of a substrate,] in the condition that the section is not formed, either, and will become processible [an anisotropy].

[0036] As for the mixed gas of the chlorine (Cl₂) used for this 2nd plasma-etching processing, and oxygen (O₂), it is desirable to choose it as within the limits whose mixing percentage of oxygen (O₂) is 0.5% thru/or 30%.

[0037] On the other hand, although the component of a mask 16 does not contain the thing which uses carbon as a principal component, or carbon, even if it uses any, the same mask function can be demonstrated, but when what does not contain the carbon which consists of silicon nitride, silicon oxide, etc. is used, selectivity with the gate oxide 14 of a substrate becomes high.

[0038] In addition, although the silicon deposition film of the semiconductor device substrate 7 which carries out plasma-etching processing by the deposition film surface-preparation approach by this invention was the example which is the monolayer of n mold polycrystalline silicon section 15 in the aforementioned explanation The silicon deposition film set as the object of the deposition film surface treatment approach by this invention What is JUARU gate membrane structure when p mold dope field where it was not restricted to the example which is the monolayer of n mold polycrystalline silicon section 15, but the deposition film doped p mold impurity, and n mold dope field which doped n mold impurity are shared, On the silicon film, a tungsten (W), nickel (nickel), cobalt (Co), What carried out the laminating of refractory metal layers, such as titanium (Ti), molybdenum (Mo), and chromium (Cr), and the layer which contains the nitride of these metals as barrier film which prevents diffusion, Or even if it is the silicon film which has the silicide of these metals, it is possible to perform plasma-etching processing similarly.

[0039] Moreover, there is no deposition film surface treatment approach by this invention, and it can make the same function attain with respect to the plasma production approach.

[0040] According to the gestalt of the above operation, it replaces with the over etching processing by the mixed gas of the high hydrogen bromide (HBr) and oxygen (O₂) of the processing pressure force currently performed conventionally. By performing over etching processing by the mixed gas of the low chlorine (Cl₂) of the processing pressure force, and oxygen (O₂) the gate oxide of residue, side etch, and a substrate -- also running -- while there is nothing and being able to perform etching processing processing of high process tolerance in an anisotropy, adhesion of the depository object to a processing room can be lessened.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the sectional view showing the outline of the configuration of the plasma etching system used for enforcing the deposition film surface-preparation approach by this invention.

[Drawing 2] In case plasma-etching processing of the silicon deposition film of a semiconductor device is carried out and n mold gate electrode pattern is obtained using the plasma etching system illustrated by drawing 1, it is the sectional view showing the change condition of n mold gate electrode pattern.

[Drawing 3] In case plasma-etching processing of the n mold polycrystalline silicon part is carried out by the known surface-preparation approach and n mold gate electrode pattern is obtained, it is the sectional view showing the change condition of n mold gate electrode pattern.

[Description of Notations]

- 1 Vacuum Housing
- 2 Microwave Installation Aperture
- 3 Flueing Opening
- 4 Electromagnet
- 5 Sample Base
- 6 Insulator Layer
- 7 Semiconductor Device Substrate (Sample)
- 8 Microwave Induction
- 9 Microwave Generation Source
- 10 High Frequency (RF) Bias Power Supply
- 12 Gas Induction
- 13 Silicon Substrate
- 14 Gate Oxide
- 15 N Mold Polycrystalline Silicon Section (N Mold Gate Electrode Pattern)
- 16 Mask

[Translation done.]

* NOTICES *

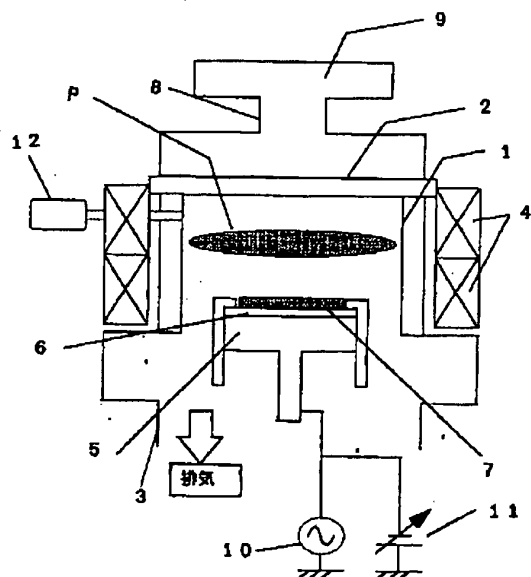
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DRAWINGS

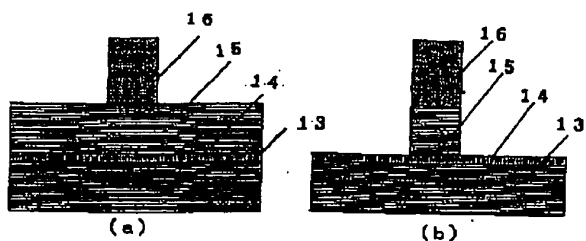
[Drawing 1]

【図 1】



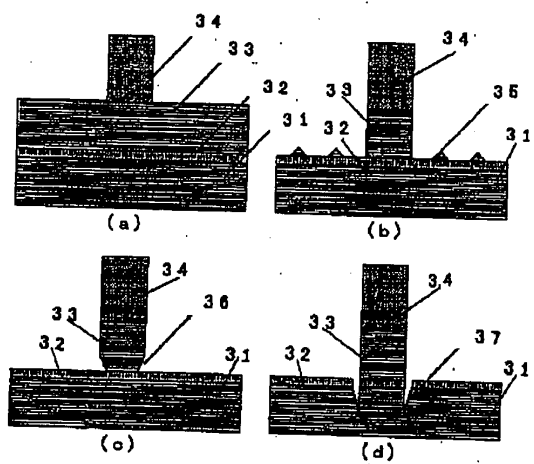
[Drawing 2]

【図 2】



[Drawing 3]

[図 3]



[Translation done.]